UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,605	04/14/2005	William A Steer	GB 020177	8232

24737 7590 07/27/2009

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
RAINEY, ROBERT R	
ART UNIT	PAPER NUMBER
2629	
MAIL DATE	DELIVERY MODE
07/27/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/531,605	STEER, WILLIAM A	
	Examiner	Art Unit	
	ROBERT R. RAINEY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 10 and 15 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

2. In the office action mailed 4/1/2009 examiner indicated that claim 8 represented allowable subject matter. This indication is withdrawn.

Some nomenclature to be used here and elsewhere in this office action: "reference voltage" the voltage applied to a first terminal of the storage capacitor during programming in order to allow the capacitor to be charged to a level reflective of "pixel voltage" minus "reference voltage" with the "pixel voltage" applied to a second terminal of the capacitor.

Examiner felt at the time of the previous office action that the change of the reference voltage used during programming by Akimoto in Fig. 13 that would be caused by disabling the current flow from the drive transistor through the display element was sufficient to make the change non-obvious even though such disabling, as such, was taught. Subsequent identification of teachings regarding the use of alternative reference voltage levels, as detailed in the rejection of claim 8 below, caused examiner to reevaluate his position.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 8, 10, 15, and 17** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites the limitations "a drive voltage being provided to the gate of the drive transistor" at 5:1, “a storage capacitor for storing a drive level” at 5:7, and “a first mode in which a pixel voltage is applied to the input to the pixel, the address transistor is turned on, the disabling means is turned on to turn off the display element and the storage capacitor is charged to a level derived from the drive voltage". It is unclear what is meant by “a drive voltage”. It is also unclear whether application of the pixel voltage and related charging of the storage capacitor to a level derived from the drive voltage does or does not describe the storing of a drive level implied in "for storing a drive level". It is further unclear whether the "level" referred to in "the storage capacitor is charged to a level" is one representative of coulombs of charge or voltage.

The problems seem to come mostly from the fact that both in the specification and in the claims applicant uses “drive voltage” imprecisely. This can be seen clearly by reference to the following portions of paragraphs from the specification, which are referred to by paragraph number as printed in the pre-grant publication by the USPTO.

> [0017] a drive transistor for driving a current through the display element, **a drive voltage** being provided to the gate of the drive transistor; and
>
> [0020] In this arrangement, a stepped signal is provided to the gate of the drive transistor so that one of the steps provides a transition between an on and off state of the drive transistor. **The drive voltage** dictates when this transition takes place, so that **the drive voltage** provides a pulse width modulation drive scheme for the drive transistor.

These passages seem to imply that “a drive voltage” comprises not just a single voltage level but all voltage levels applied to the gate of the drive transistor. Examiner will refer to this sense as “drive waveform”. (Note that examiner recognizes that this could also be a poorly worded attempt to embody the "stored voltage" sense below.)

> [0046] FIG. 3 shows a first pixel arrangement in accordance with the invention. As in the conventional pixel of FIG. 2, the pixel is voltage-addressed, by applying a gate **drive voltage** to the drive transistor 22.

This seems to imply that the “drive voltage” is the voltage stored on the capacitor as in the prior art. Examiner will refer to this sense as “stored voltage”. Applicant seems to have called this sense “a drive level” in the claim.

> [0049] During this programming stage, the *column conductor 6* is held to a **drive voltage** (lower than the power supply line voltage) so as to charge the capacitor to the desired voltage.
>
> [0052] FIG. 4 is used to explain in greater detail the operation of the circuit.
>
> [0053] The pixel drive scheme starts with the programming phase. Plot 40 shows the voltage on the address line 33. During the programming phase, the address line voltage is switched low in order to turn on the PMOS address transistor 32. The capacitor 30 is then charged through the address transistor 32 to a voltage dependent on the voltage provided on the *column 6*. Plot 42 shows the voltage provided on the column, and the part 42a of the plot is the **pixel drive level** having a step height shown as 46, which determines the voltage stored across the capacitor 30. During the programming phase, the isolating transistor is turned off, and

> plot 44 shows the voltage on the enable line 36. The low voltage during the programming phase turns off the NMOS isolating transistor 34.

"drive voltage" in [0049] and "pixel drive level" in [0053] seem to refer to the same thing, which is the voltage applied to the terminal of the capacitor connected to the column conductor during programming. Examiner will refer to this sense as "pixel drive level". Applicant seems to have called this sense "a pixel voltage" in the claim.

Note that, according to examiner's understanding of applicant's disclosure as a whole, neither the "stored voltage" nor the "pixel drive level" is ever applied to the gate of the drive transistor, except perhaps transiently. The voltages "provided to the gate of the drive transistor" are

"pixel drive level" plus a previously stored "stored voltage",

V_{SUPPLY},

V_{SUPPLY} plus the currently stored "stored voltage", and

step level plus the currently stored "stored voltage".

Since two of the senses, "stored voltage" and "pixel drive level", seem to be alternatively referred to in the claim and neither is "provided to the gate of the drive transistor", the only sense of "drive voltage" remaining is "drive waveform" but it would be a circular reference to have the voltage on the capacitor, which is used to generate the drive waveform, be derived from the drive waveform. And, it is unnecessarily confusing and certainly non-standard usage to refer to a waveform comprising various voltage levels as "a drive voltage".

Claim 10 recites the limitation "avoiding a linear operating region of the drive transistor by having a height of the first set of the voltage steps being greater than a voltage width of the linear operating region of the drive transistor". It is unclear whether a particular transition between voltage levels belongs to the first or second set. See for example Fig. 4 and consider: are there two or three transitions associated with the "on" steps.

Claim 15 recites the limitations:

> "disabling the driving of the current by the drive transistor through the display element during the storing of a pixel drive level on the storage capacitor;
>
> in a first mode in which a pixel voltage is applied to the input to the pixel, turning on the address transistor, turning off the display element, and charging the storage capacitor to a level derived from the drive voltage;"

It is unclear whether the two indented phrases refer to the same or different sets of acts.

Claim 17 recites the limitations:

> "wherein the stepped voltage waveform to the input of the pixel has the same voltage levels in the two phases, and the shorter phase has shorter step transitions."

The language does not compel absolute clarity as to whether the "transitions" are transitions in time or voltage. A waveform having the same voltage levels could mean a waveform of any shape that encompasses the same minimum to maximum levels. The use of "step transition" to refer to the time during which the voltage is held constant, which seems most likely given applicants disclosure, seems contrary to customary usage in which a step transition would

refer to the short duration transition of voltage levels that occurs between one held voltage level and the next.

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 10 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 10 includes the limitation "a height of the first set of the voltage steps being greater than a voltage width of the linear operating region of the drive transistor". Claim 11, which depends from claim 10 states "wherein the height of the steps in the stepped voltage waveform is greater than the voltage width of the linear operating region of the drive transistor". In order for claim 10 to encompass more than claim 11, claim 10 must read on an embodiment in which the height of at least one of the second set of voltage steps is not greater than a voltage width of the linear operating region of the drive transistor. Such an embodiment was not described in the disclosure as filed.

Claim 10 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter

which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 10 includes the limitation "a height of the first set of the voltage steps being greater than a voltage width of the linear operating region of the drive transistor". Claim 11, which depends from claim 10 states "wherein the height of the steps in the stepped voltage waveform is greater than the voltage width of the linear operating region of the drive transistor". In order for claim 10 to encompass more than claim 11, claim 10 must read on an embodiment in which the height of at least one of the second set of voltage steps is not greater than a voltage width of the linear operating region of the drive transistor. Such an embodiment was not described in the disclosure as filed nor does it seem that the manner of implementing such an embodiment would be obvious.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

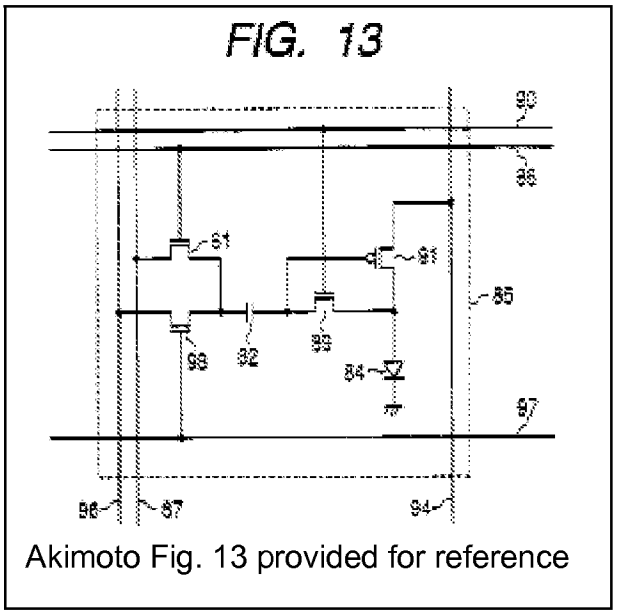
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 1-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,876,345 to *Akimoto et al.* ("*Akimoto*") in view of U.S. Patent No.

6,188,375 to *Kagey* ("*Kagey*") and further in view of "PIXEL-DRIVING METHODS FOR LARGE-SIZED POLY-SI AM-OLED DISPLAYS" by A. YUMOTO et al. ("*Yumoto*").

As to **claim 8**, *Akimoto* sixth embodiment discloses:

an active matrix electroluminescent display device comprising an array of display pixels (see for example column 5 lines 5-10 and column 1 lines 36-42), each pixel comprising:



Akimoto Fig. 13 provided for reference

an electroluminescent display element (see for example Fig. 13 item 84 and column 12 line 35);

a drive transistor (see for example Fig. 13 item 91 and column 12 lines 30-36) for driving a current through the display element, a drive voltage being provided to the gate of the drive transistor (the drive transistor is disclosed to be voltage responsive, see for example Fig. 14 especially "PIXEL DRIVING VOLTAGE");

an address transistor, connected between a power supply line and the gate of the drive transistor (see for example Fig. 13 item 89; note that the connection to "a power supply line" is met for any of the following reasons: the node to which transistor is directly connected can supply power, the node to which the transistor is directly connected provides a desired reference voltage, the transistor connects to p-channel source line 94 through transistor 91, the transistor connects to ground through diode 84);

~~means for disabling the driving of the current by the drive transistor through the display element;~~ and

a storage capacitor (see for example Fig. 13 item 82 and column 12 lines 25-30) for storing a drive level (see for example "signal voltage" of Fig. 14 and column 12 lines 51-55), said storage capacitor being connected between an input to the pixel and the gate of the drive transistor (see for example Fig. 13, which shows the capacitor so connected),

wherein a driver circuitry provides a ~~stepped~~ voltage waveform to the input of the pixel, the ~~stepped~~ voltage waveform being voltage-shifted by the storage capacitor before application to the gate of the drive transistor~~, and wherein the height of the steps in the stepped voltage waveform is greater than the voltage width of the linear operating region of the drive transistor~~, wherein the device is operable in two modes:

a first mode in which a pixel voltage (see for example Fig. 5 "SIGNAL VOLTAGE") is applied to the input to the pixel, the address transistor is turned on

(see for example Fig. 5, "RESET LINE" "ON" corresponds to the address transistor turned on~~), the disabling means is turned on to turn off the display element~~ and the storage capacitor is charged to a level derived from the drive voltage (for purposes of examination examiner will read "drive voltage" as "pixel voltage" as this is the input that is changed to vary the level to which the capacitor is charged; see the 35 U.S.C. 112, second paragraph, rejection of claim 8 for further insight into examiner's reasons for changing the wording in order to allow examination); and

a second mode in which the address transistor is turned off,~~ the disabling means is turned off~~ and the stepped voltage waveform is applied to the input of the pixel (see for example Fig. 5 "DRIVING PERIOD").

Akimoto third embodiment discloses that the voltage waveform is stepped and that the height of the steps in the stepped voltage waveform is greater than the voltage width of the linear operating region of the drive transistor so that the linear operating region of the drive transistor is avoided (see for example Fig. 10 and column 9 line 57 to column 10 line 21, noting that the inverter and thus the drive transistor, i.e. item 31 or 32 of Fig. 6, is off at one step and on at another, and further that setting the writing signal at a medium level ensures that the switch point, i.e. linear operating region, is crossed in the transition from one step to another; since this is indicated as a stepped transition the linear operating region is "avoided", that is the transition through this region is rapid; note that the

underlined language from claim 1 is included in this rejection because each of the other independent claims include a version of an avoided region limitation).

Akimoto sixth embodiment and *Akimoto* third embodiment are analogous art because they are from the same field of endeavor, which is image displays capable of multilevel display, and seek to solve the same problem, which is to reduce the variation in PWM circuits caused by differences between TFT circuitry.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to apply the stepped waveform of *Akimoto* third embodiment to the circuit of *Akimoto* sixth embodiment. The suggestion/motivation would have been to provide advantages such as to prevent changes caused by noise (see for example column 10 lines 11-14).

Examiner remains of the opinion that the teachings of Akimoto are sufficient to have reasonably suggested to one of ordinary skill in the art making the height of the steps larger than the width of the linear operating region of the drive transistor in order to avoid a linear operating region of the drive transistor. However, in order to provide a yet clearer teaching, examiner combines *Kagey* with *Akimoto*.

Kagey discloses a pixel drive circuit and method for active matrix electroluminescent displays that has a different circuit configuration but operates in much the same manner as does *Akimoto*, i.e. PWM illumination achieved by storing an offset voltage on a capacitor that shifts the voltage of an applied

stepped voltage ramp such that the drive transistor is turned on or off at a desired step (hereinafter referred to as “the driving method”). In particular, the height of the steps in the stepped voltage waveform being greater than the voltage width of the linear operating region of the drive transistor in order to avoid the linear operating region of the drive transistor is taught (see for example Fig. 3 and Fig. 6 and 1:23-25 "The pixels in a conventional AMEL display are either active (illuminated) or inactive (dark) at any given time. To generate shades of gray, typical AMEL displays are operated in a time multiplexed mode." and 2:24-37 especially “…all of the transistors in the AMEL driver circuit of FIG. 2 must consistently *respond* to a small change in voltage… However, … not … sufficient uniformity … to support this requirement. Therefore, the step size must be increased either by using non-conventional power supply voltages or by reducing the number of gray scale steps of the display”, since the response required is on-to-off/off-to-on the width of the linear region is that which is talked about; and 6:43-48 especially, “By using such relatively course steps, sufficient margins are maintained between profile states to insure that any non-uniformity in the AMEL display does not adversely affect the illumination characteristics of the display.”).

Akimoto sixth embodiment and *Akimoto* third embodiment, hereinafter *Akimoto_C*, and *Kagey* are analogous art because they are from the same field of endeavor, which is image displays capable of multilevel display, and seek to solve the same problem, which is to reduce the variation in PWM circuits caused by differences between TFT circuitry.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to make the height of the steps in the stepped voltage waveform of *Akimoto_C* greater than the voltage width of the linear operating region of the drive transistor in order to avoid the linear operating region of the drive transistor as taught by *Kagey*. The suggestion/motivation would have been to provide advantages such as to reduce power dissipation in the drive transistor.

Kagey further discloses that the reference voltage may be ground (see for example Fig. 4) and reasonably suggests by extension that it may be any voltage connected to the source or drain of the drive transistor and further discloses or reasonably suggests that the reference voltage may be any desired voltage (see for example Fig. 3 and 4:12-14 especially "During a load cycle, the profile voltage terminal 314 is held at an initial voltage.").

Yumoto discloses a number of pixel driving circuits for OLED displays with at least two (Fig. 2 and 3) being circuits that store a voltage level on a capacitor and include a transistor (T4) that shuts of current flow through the drive transistor to the display element while the voltage level is stored, i.e. disabling means turned on in first mode, and conversely allows the current to flow through the drive transistor to the display element during a driving period, i.e. disabling means turned off in second mode. While, not specifically discussed, it is reasonably suggested to one of ordinary skill in the art at the time of the invention that at least one of the functions of this transistor is to prevent the OLED from illuminating during the storing of the voltage level.

Akimoto_C and *Kagey* and *Yumoto* are analogous art because they are from the same field of endeavor, which is OLED displays.

Thus the prior art contains a base device, *Akimoto_C* and *Kagey*, upon which the claimed invention can be seen as an improvement. This because *Akimoto_C* and *Kagey* allows current flow through the OLED from the drive transistor during storage of a voltage on the storage capacitor. We see that the prior art contained comparable devices, the pixel circuits of *Yumoto*, that have been improved in the same way as the claimed invention. One of ordinary skill in the art at the time of the invention could have applied the known improvement to the device of *Akimoto_C* and *Kagey* and the results would have been predictable to one of ordinary skill in the art, that is the current flow through the OLED during voltage level storage would be substantially eliminated and the reference voltage would change from that of *Akimoto_C* and *Kagey* to a voltage of the threshold voltage drop of the drive transistor below the voltage on line 94. The conclusion that the change in the reference voltage would have been obvious to one of ordinary skill in the art is supported by the fact that this reference voltage level was taught in *Yumoto* Fig. 2 and *Akimoto* Fig. 17. The conclusion that any changes required to allow the circuit to function with the changed reference voltage would have required no more than ordinary skill in the art is supported by the fact that *Kagey* taught or reasonably suggested the use of any reference voltage or that *Akimoto* taught at least two different reference voltage levels (compare for example Fig. 13 and Fig. 12).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to provide means for disabling the driving of the current by the drive transistor through the display element with the disabling means turned on in the first mode and turned off in the second mode as taught by *Yumoto* as a modification of the device after *Akimoto_C* and *Kagey*.

Claims 1, 4, and 5 claim a subset of the limitations of claim 8 and are rejected on the same grounds and arguments as claim 8.

As to **claim 2**, in addition to the rejection of claim 1 over *Akimoto_C, Kagey* and *Yumoto*, *Kagey* further discloses or reasonably suggests that the height of the steps in the stepped voltage waveform is sufficient to include the linear operating region voltages of the drive transistors of all pixels of the display (see for example 2:24-37 especially "…sufficient uniformity across the AMEL display substrate…").

Akimoto_C further discloses that the drive level is selected to have one of a plurality of values, and is selected such that any gate voltage for the drive transistor in the linear region corresponds to a voltage between steps of the voltage applied to the gate of the drive transistor (note that Fig. 10 shows two different stored levels and that each of these is set at a midpoint between step levels; further see for example 10:15-21).

As to **claim 3**, in addition to the rejection of claim 1 over *Akimoto_C, Kagey* and *Yumoto*:

Akimoto_C further discloses that the drive level is selected to have one of a plurality of values, and is selected such that any gate voltage for the drive transistor in the linear region corresponds to a voltage between steps of the voltage applied to the gate of the drive transistor (note that Fig. 10 shows two different stored levels and that each of these is set at a midpoint between step levels; further see for example 10:15-21).

Kagey further discloses that the drive level is selected to have one of a plurality of values, and is selected such that any gate voltage for the drive transistor in the linear region corresponds to a voltage between steps of the voltage applied to the gate of the drive transistor (see for example Fig. 6 shows six different levels that imply six different stored levels; the fact that the transistor is either on or off at a particular step, see for example previous citations, means that the linear region corresponds to a voltage between steps).

As to **claim 6**, in addition to the rejection of claim 5 over *Akimoto_C, Kagey* and *Yumoto*: the limitation that the means for disabling comprises an isolating transistor in series with the drive transistor and the display element was already covered in the rejection claim 1 from which claim 6 depends.

As to **claim 7**, in addition to the rejection of claim 4 over *Akimoto_C, Kagey* and *Yumoto*: *Akimoto_C* further discloses disabling means comprising a switch for switching the voltage on one terminal of the display elements of the array of pixels (see for example Fig. 13 item 89). To further prosecution examiner also notes that a power switch for the device would also read on the claim limitation as written.

As to **claim 7**, in addition to the rejection of claim 4 over *Akimoto_C, Kagey* and *Yumoto*:

Examiner takes official notice that disabling means comprising a switch for interrupting a common path through which a voltage is supplied in parallel to a group of display elements by connection to one terminal of each display element of the group of display elements of the array of pixels in order to avoid lighting of the elements during programming was well known. The most common version of this is a switch in the ground return path of the OLEDs. It can be thought of as a rearrangement of parts with known advantages and disadvantages compared to a switch per element.

As to **claim 9**, in addition to the rejection of claim 1 over *Akimoto_C, Kagey* and *Yumoto*:

Akimoto_C further discloses that the device is operable to provide pulse width modulation (see for example 3:34-4:27).

Kagey further discloses the device is operable in at least two sequential phases, one phase providing coarse resolution pulse width modulation (see for example Fig. 6C the fourth and fifth steps from the left) and the other, shorter phase, providing fine resolution pulse width modulation (see for example Fig. 6C the first three steps from the left).

Claim 10 claims the method implicit in the apparatus of claim 8 with additional limitations that will be addressed below and is rejected on the same grounds and arguments as claim 8 with the following additions.

Akimoto_C further discloses that for a first set of the voltage steps applied to the gate of the drive transistor, the drive transistor is turned on, and for a second set of the voltage steps applied to the gate of the drive transistor, the drive transistor is turned off, the first and second sets being determined by the stored pixel drive level (see for example Fig. 10 and column 9 line 57 to column 10 line 21, noting that the inverter is on for period corresponding to a first set of steps indicated as being part of the "COLUMN ILLUMINATING PERIOD" and off for the rest or second set of steps).

As to **claim 11**, in addition to the rejection of claim 10 over *Akimoto_C, Kagey* and *Yumoto*:

The limitation that the height of the steps in the stepped voltage waveform is greater than the voltage width of the linear operating region of the drive

transistor was covered by the rejection of claim 10 since this was a limitation included in claim 8.

As to **claim 12**, in addition to the rejection of claim 11 over *Akimoto_C, Kagey* and *Yumoto*:

Kagey further discloses or reasonably suggests that the height of the steps in the stepped voltage waveform is greater than the voltage width of the overlaid linear operating region voltages of the drive transistors of all pixels of the display (see for example 2:24-37 especially "…sufficient uniformity across the AMEL display substrate…").

Ref: claim 2

As to **claim 13**, in addition to the rejection of claim 10 over *Akimoto_C, Kagey* and *Yumoto*:

Akimoto_C further discloses that the drive level is selected to have one of a plurality of values, and is selected such that any gate voltage for the drive transistor in the linear region corresponds to a voltage between steps of the voltage applied to the gate of the drive transistor (note that Fig. 10 shows two different stored levels and that each of these is set at a midpoint between step levels; further see for example 10:15-21).

Kagey further discloses that the drive level is selected to have one of a plurality of values, and is selected such that any gate voltage for the drive transistor in the linear region corresponds to a voltage between steps of the

voltage applied to the gate of the drive transistor (see for example Fig. 6 shows six different levels that imply six different stored levels; the fact that the transistor is either on or off at a particular step, see for example previous citations, means that the linear region corresponds to a voltage between steps).

Ref: claim 3

As to **claim 14**, in addition to the rejection of claim 10 over *Akimoto_C, Kagey* and *Yumoto*: the limitation that the act of storing a pixel drive level on the storage capacitor comprises turning on an address transistor connected between a power supply line and the gate of the drive transistor and charging the storage capacitor using the address transistor was covered in the rejection of claim 8, which was the starting point for the rejection of claim 10 from which claim 14 depends.

As to **claim 15**, claim 15 is rejected on the same grounds and arguments as claim 10. All limitations of claim 15 were covered in the rejection of claim 10 since equivalents of the limitations from claim 15 missing from claim 10 are in claim 8, which was the starting point for the rejection of claim 10.

Ref: claims 11 and 14

As to **claim 16**, in addition to the rejection of claim 1 over *Akimoto_C, Kagey* and *Yumoto*:

Akimoto_C further discloses that the device is operable to provide pulse width modulation (see for example 3:34-4:27).

FIRST MAPPING

Kagey further discloses a device operable in at least two sequential phases, one phase providing coarse resolution pulse width modulation (see for example Fig. 6C the fourth and fifth steps from the left) and the other, shorter phase, providing fine resolution pulse width modulation (see for example Fig. 6C the first three steps from the left).

SECOND MAPPING

Since the combination of *Akimoto_C, Kagey* and *Yumoto* described so far does not confine the device to a single speed of operation, i.e. step length, it is reasonable to assume that it may be operated at two or more speeds, i.e. one faster and thus having shorter pulses or finer resolution. Since it is operable at two speeds it is operable in at least two sequential phases at the two different speeds, i.e. at course and fine resolution pulse width modulation speeds.

Ref: claim 9

As to **claim 17**, in addition to the rejection of claim 16 according to the SECOND MAPPING over *Akimoto_C, Kagey* and *Yumoto*:

Note that the mapping of the at least two sequential phases is changed below.

Kagey further discloses a device operable in at least two sequential phases in which the at least two sequential phases are used to generate a desired gray scale (see for example Fig. 6 with a PASS representing a phase) that provides coarse resolution pulse width modulation (see for example Fig. 6C the fourth and fifth steps from the left) and fine resolution pulse width modulation (see for example Fig. 6C the first three steps from the left) and the stepped voltage waveform to the input of the pixel has the same voltage levels in the two phases (see for example Fig. 6).

It would have been obvious to one of ordinary skill in the art at the time of the invention to improve the device of *Akimoto_C, Kagey* and *Yumoto* to use at least two sequential phases to generate the desired gray scale as taught by *Kagey* while continuing to use a uniform step length within each sequence of steps as taught by *Akimoto_C* and providing for different step lengths, i.e. course and fine resolution PWM steps, within the series of sequential phases as taught by *Kagey*.

The suggestion/motivation would be to provide advantages such as to increase step size for a given resolution of gray scale operation (see for example *Kagey* 2:49-50) or to simplify the step size generation.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 5,302,966 provides an early example of the driving method.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT R. RAINEY whose telephone number is (571)270-3313. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RR/

/Amare Mengistu/

Supervisory Patent Examiner, Art Unit 2629